National Semiconductor

The GeodeLink™ System Architecture

The information appliance is the next evolution for personal computing. Thin clients, set top boxes and Webpad™s require optimization of the entire system architecture. Information appliances require high levels of integration to reduce power, cost and to provide optimal system performance. At the same time, the information appliance requires software compatibility with existing systems to allow new software to evolve from the existing PC infrastructure.

PC system architectures have evolved into a handful of discrete components with multiple memory interfaces and a variety of interconnect buses. These interconnects have physical and logical limitations due to the board level interconnects, cost optimizations and legacy designs. While perishable processors and multiple memory interfaces meet the market needs for PCs, they do not provide the optimal performance, cost and power for the next generation of information appliances.

The GeodeLink system architecture is a top to bottom system architecture for National Semiconductor's information appliance system on a chip. It provides an evolutionary software model for compatability, while providing a revolutionary jump in on-chip interconnect performance. This enables the next step in cost and power saving while providing optimal performance in an information appliance. The key features of the GeodeLink system architecture are as follows:

- High performance on-chip switched fabric
  - Pipelining of multiple read and/or write requests from various devices
  - Out-of-order data streams
  - Extensible to a variety of bus widths (from 16 to 256 bits) and clock rates (33-300 MHz)
  - Various access sizes (1 to 32 bytes)
  - Standard bridges to legacy buses (PCI, ISA)
  - Peer-to-peer communication
  - Cache snooping and write-back
  - Physical to physical address translation
- Optimized Unified Memory Architecture (UMA)
  - Frame buffer display compression
  - Advanced arbitration for real-time and isochronous devices
  - Speculative arbitration for low latency transactions
- Standard GeodeLink software model
  - Active Hardware Power Management (AHPM)
  - GeodeLink virtual PCI system architecture
  - Full x86 compatibility
- On-chip development support
  - Standard diagnostic and test interface
  - Branch Trace Messaging (BTM)
  - Third party debugger support

GeodeLink Concept

The GeodeLink system architecture provides a layered chip infrastructure that begins with a signal interface and layers diagnostics, power management, software, design verification and floor planning on top of a simple common starting point. Figure 1 illustrates the GeodeLink System Architecture layered foundation.

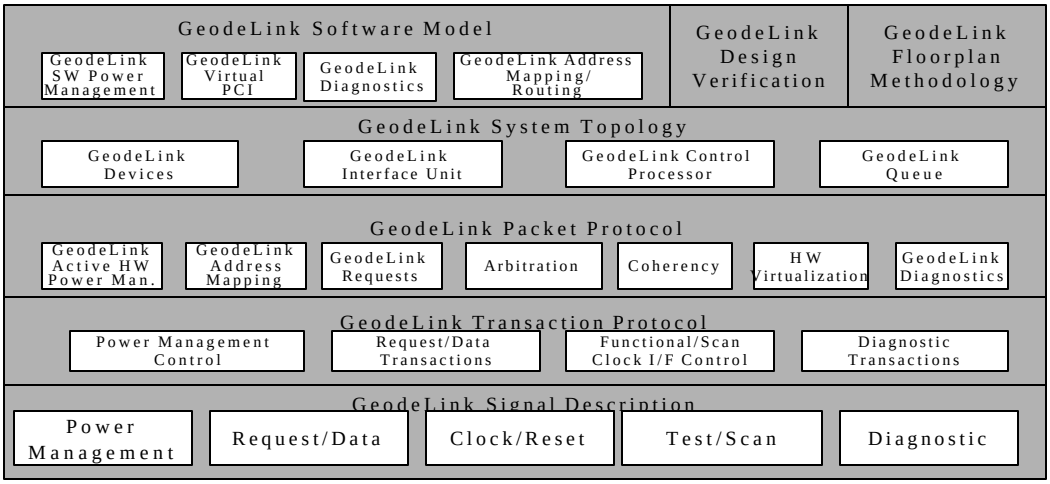

Figure 1. GeodeLink™ system architecture layers

The foundation for the GeodeLink architecture is the standard signal description. A GeodeLink device initiates and services requests via 4 bus interfaces: 2 request buses and 2 data buses. The request bus contains address, byte enables (32-bit or 64-bit reads), cycle type, and routing information for transactions. The data bus contains data, byte enables (for writes), write completion status, and routing information to associate the data bus packets with the appropriate request bus packet. The busses are unidirectional and point-to-point to minimize loading and timing variations. In addition, the GeodeLink signals provide a diagnostic bus, power management controls, clocks, reset and a scan interface.

The GeodeLink transaction protocol defines the mechanism for transferring packets between GeodeLink devices. In addition, the transaction protocol defines the control for clocks and power management.

The GeodeLink packet protocol standardizes the system level interactions between GeodeLink devices. The packet protocol orders all transactions in the system, arbitrates packets, maintains coherency, and routes transactions to their destinations.

The GeodeLink system topology consists of basic GeodeLink building blocks which can be connected in various configurations. The major building blocks are the following:

- GeodeLink Device – a piece of GeodeLink IP that maintains the GeodeLink protocol
- GeodeLink Bus Interface Unit (GLIU) – performs GeodeLink packet protocol and connects GeodeLink devices
- GeodeLink Queue (GQ) – A queue that bridges GeodeLink ports with different widths and/or frequencies
- GeodeLink Control Processor (GCP) – GeodeLink Device that performs clock control, power management control, and diagnostic features

These building blocks can attach in a variety of configurations to provide different topologies. Figure 2 demonstrates a possible topology.

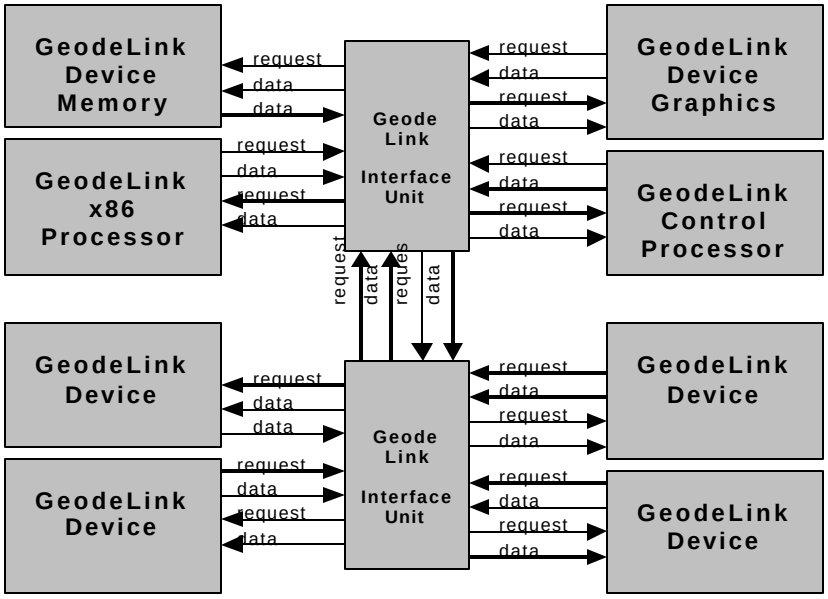

Figure 2. GeodeLink™ interconnect topology

The GeodeLink system architecture is visible to software via the GeodeLink software model. GeodeLink devices appear to OS and driver level SW as PCI devices. Thus, there are no application or driver level code changes needed for GeodeLink devices. In addition, GeodeLink provides active hardware power management for OS independent power management.

GeodeLink On-chip High Performance Switched Fabric

The GeodeLink high performance switched fabric ensures that the interconnect is never the bottleneck. First, the integration of all components on a single chip provides very low latency transactions for latency critical devices. Integration provides opportunities to remove physical bottlenecks between devices. Wide unidirectional buses, synchronous clocking, and close physical placement reduce latency and power in a system.

All GeodeLink devices are equal peers. Thus, any device can talk to any other devices at peak bandwidths simultaneously. High performance peer-to-peer transactions are optimal for streaming video and video decoding by minimizing memory transactions and buffering. The GeodeLink interface units perform multiple request and data transactions per cycle at clock rates up to 300 MHz. This provides an on chip BW of more than 6 Gbytes/s. Streaming devices maintain peak bandwidth with up to 31 outstanding transactions per devices. Thus, the number of outstanding transactions is never a bottleneck.

Each GeodeLink device has a private connection to the interconnect. Up to 7 devices can attach to a GeodeLink Interface Unit (GLIU). The GLIU contains the arbiter and routing tables and maintains all the GeodeLink ordering rules. Multiple GLIU can be attached to form hub and spoke networks distributed throughout the chip. This allows up to 64 GeodeLink devices to be connected in a system.

GeodeLink Optimized Unified Memory Architecture

GeodeLink is optimized for Unified Memory Architecture (UMA) systems. UMA implementations save system cost and power at the expense of some performance. The GeodeLink optimized UMA uses

advanced arbitration, memory controller optimizations, and display compression to increase the performance of a UMA system.

The GeodeLink™ system architecture uses a proprietary arbitration algorithm to balance real time data streams, low latency streams, and high bandwidth streams. The arbitration allows devices to provide instantaneous priority information. The GLIU can then determine the most important transactions to execute and maintain fairness. When a device increases priorities, the entire data stream inherits the new priority.

Arbitration latencies are greatly reduced using speculative arbitration to guess the destination of a transaction in advance. The GLIU performs address decode, ordering rules and arbitration in parallel. If the destination guess is correct, the arbitration is successful and the request is transmitted in 1 cycle. If the guess is incorrect, one extra cycle is consumed for arbitration. Typical destination guess rates are above 99%.

Using out-of-order transactions, all the data streams can be reordered by a slave device to ensure the most efficient execution of the requests. This enables the GeodeLink memory controller to perform advanced optimizations to minimize read/write turn arounds and row changes and to reorder transactions based on priorities.

The GeodeLink architecture also uses display buffer compression to reduce the bandwidth to main memory. Display streams can range in bandwidth from 20-300MB/s and consume as much as 30-40% of the total available memory bandwidth. Therefore, the GeodeLink architecture supports display buffer compression to reduce the bandwidth by as much as 10:1. This allows for more optimal processor performance by reducing the total system bandwidth requirements. In addition, the reduced bandwidth allows customers to use either slower or narrower memory buses for a given application. Reduced memory requirements save both system cost and power.

Standard GeodeLink Software Model

The GeodeLink software model maintains compatibility with existing x86 and PCI based systems, while also enhancing the software model to provide OS independent power management and expose the advanced GeodeLink features.

The virtual PCI system architecture allows PCI based drivers and software to run seamlessly on a GeodeLink device. The GeodeLink system architecture has a non-standard bus architecture and requires different software configurations than a PCI system. All the PCI configuration cycles are trapped and emulated providing a complete PCI software model. The trapped PCI configurations are then turned into GeodeLink configurations. The virtual PCI system architecture hides all of the GeodeLink address maps and configuration code from the application, OS, and driver.

Since the GeodeLink software model is compatible with the x86 system architecture, it is compatible with all the legacy features of a PC system including ISA and PCI legacy devices. In addition, all future GeodeLink products will be compatible with x86 systems.

The GeodeLink system architecture provides active hardware power management (AHPM) for operating system independent power management. There is currently no standard power management model for information appliances. There are simply to many operating systems and no unifying standard. AHPM is fully compatible with ACPI and APM when available. However, for all the other operating systems, AHPM provides power management without OS interaction. The AHPM model uses the x86 system management mode in conjuction with GeodeLink power management hardware to perform all levels of system power management. This enables customers to have quick access to power management without modification to drivers and applications. The AHPM software model supports user plug-in extensions.

AHPM uses transaction based power management at the to manage power at the device level during active processing. Transactions on device I/O or GeodeLink interfaces wake up the hardware without software

interaction. The devices monitor their own activity and determine when to move into more power friendly states. This enables the devices to precisely control their power consumption.

GeodeLink™ On-chip Development Support

Integrated information appliances create new challenges for development and debug of software. Buses and interfaces that are visible in a nonintegrated system are embedded in the silicon. This reduces the visibility of internal events in the system. As the integration trend moves forward, visibility will be even further reduced.

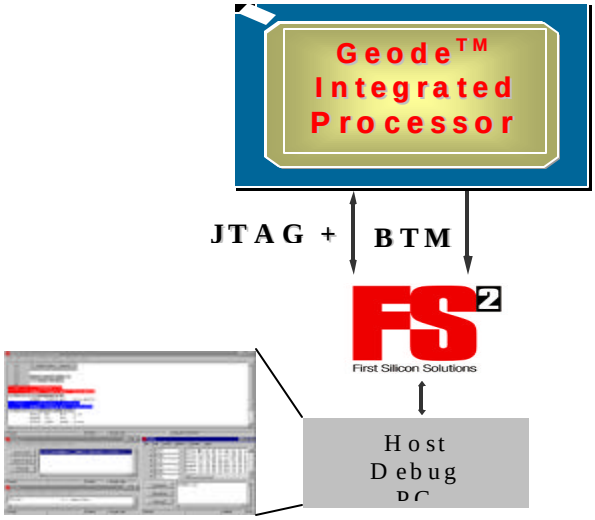

Figure3. GeodeLink™ integrated processor development environment.

The GeodeLink development environment is a full featured integrated processor development environment for both processor and peripheral debug. The development features shown in Figure 3 are accessed using an expanded JTAG port and sideband signals. The expanded JTAG port is exposed using a device from our third party partners, FS2 Inc, as a middleware layer. This enables third party debuggers to examine processor state, follow program execution and provides Branch Trace Messaging (BTM). Users can set breakpoints or stop the chip on a clock via many internal events in the processor and the peripherals.

In addition, the JTAG port is a full GeodeLink master. Via the JTAG port a user can preload memory, read or write any register in the system, and examine scan chain state. This provides complete access to the entire chip state for debug.

Summary

The GeodeLink system architecture is a revolutionary advance in on-chip interconnect for information appliances. At the same time, it provides an evolutionary advance in the software model. The GeodeLink high performance switched fabric provides enough bandwidth and performance for the next generations of information appliance. The optimized UMA reduces system cost by removing extra memory, and optimizing transaction execution. The software model provides compatibility with x86 and PCI system architectures and provides OS independent power management. The GeodeLink system architecture provides the next step in advanced development environments for highly integrated processors. These features enable National Semiconductor and our customers to provide the optimal cost, power and performance optimization for information appliances.

For more information please visit http://ia.national.com/GeodeLink